All-optical packet synchronizer for slotted core/metropolitan networks

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In the framework of synchronous optical packet networks, a cost-effective all-optical synchronizer is an important building block to effectively switch the packets through an optical router. In striking difference to its time-division multiplexing-based electronic counterparts requiring bit level synchronization, an optical router can operate effectively with a much coarser synchronization at packet level. Such a synchronizer is proposed, which can compensate for the time variations between packets transported over several wavelengths. The requested synchronization is achieved with a resolution that is a fraction of the packet duration, which is a process that is adequate to compensate for the delays due to thermal variations between the transport fibers. Because this WDM synchronizer is constructed using slowly reconfigurable and mainly passive components, it is potentially a cost-effective solution. The principle of operation of this synchronizer is described in the context of synchronous slotted optical networks; the functionality of the various building blocks is analyzed, and practical implementation issues of various subsystems for a 80 Gbit/s synchronizer are discussed. Finally, an experimental validation of the proposed synchronizer is made demonstrating the viability of the method.

1. Introduction

It is widely accepted that the traffic spanning the emerging data-centric metropolitan and wide-area networks (WANs) exhibit a bursty profile. To accommodate this traffic, either systems allowing for WDM channel overprovisioning need to be deployed, or the optical layer has to become dynamically reconfigurable [1–3]. Optical packet switching is a prominent solution for materializing the latter due to the attainable statistical multiplexing gains and, thus, reducing the hardware resources needed to construct the corresponding systems. However, all-optical packet switching concepts are inextricably linked to the deployment of viable and cost-effective optical packet routers. Toward this end, with multiterabits per second capacity optical packet routers, have already been proposed and demonstrated [1,4].

An important building block of any router in a synchronous slotted network architecture, like [1], is an optical synchronizer. This allows all incoming packets to be synchronized to a local clock, while the switching matrix is reconfigured at a steady rate. This reduces the complexity of the switch’s control plane and makes the solution viable; otherwise, the switch either has to reconfigure at a very high rate or drop packets/slots that arrive asynchronously. In the quest for cost-effective solutions, systems that scale in the multiterabits per second regime, optical transparency is an essential asset and, thus, there is a clear incentive to achieve synchronization using all-optical means.

In this paper, the concept of such an all-optical packet synchronizer is elaborated, and the functionality of the various building blocks is presented along with the demonstration of a rack-mounted prototype whose performance in terms of bit error rate (BER) is analyzed.

2. Novel Optical Synchronizer: Principle of Operation

In principle, packet synchronization could be implemented with an accuracy that is a fraction of the bit duration. This is a necessity in all concepts emulating the mode of
operation of large IP routers using the time-division multiplexing (TDM) legacy. In practice, this is a formidable task if this is to be done in the optical domain owing to the absence of the optical equivalent of RAM. In this paper, the proposed optical synchronization is developed under a different mindset in accordance with [1,2]. After this approach, any bit-by-bit optical processing of packets is avoided while these are in transit. In [1,2] only packet-level synchronization is necessary when the packets are traveling through the optical cloud, while synchronization at the bit level is performed at the receiving end with the deployment of a burst mode receiver [1,5]. This means that a tight synchronization is not a strict necessity, and the only restriction placed is that the total accumulated jitter should be less than the duration of the guard band between two consecutive packets. At the same time, it should not escape our attention that the requested multiterabits-per-second capacities can be met only though a proper exploitation of WDM. As a result a synchronizer able to handle an entire WDM comb [6] offers a competitive cost advantage. Toward this end, the challenge is to construct such a synchronizer using low-cost components.

A schematic diagram of the proposed synchronizer is shown in Fig. 1 [7], and it comprises two parts: the coarse part and the fine part. The former operates in a WDM regime and serves for compensating the fluctuations in the arrival times between different frames propagating in a WAN. Since the distance between nodes are fixed, the role of the coarse synchronizer is to (a) synchronize the slot-trains from different input fibers with respect to a local clock that is locked to the nominal slot generation rate, which for the router in [1] is 1 µsec, and (b) to dynamically readjust this condition since, due to thermal effects, there might be fluctuations in the arrival rate of slots (these are probabilistic and slowly varying phenomena in the range of a few seconds). In this work, the synchronizer is dimensioned to accommodate the router in [1].

The coarse synchronizer consists of two identical branches that comprise a cascade of slow switches and fiber delay lines (FDLs). One branch is always active, while the other in a standby mode. The synchronizer operates in a traveling mode, and no recirculation loops are implemented. At the starting point, the active branch (e.g., branch-1) is set at an arbitrary initial delay allowing the electronic control circuitry to evaluate the phase difference between the arrival time of a slot-array with respect to a local packet generation clock rate. The necessary compensation scheme is calculated, and the changes are applied to the standby branch (branch-2). Then, the semiconductor optical amplifier (SOA) of branch-1 is switched OFF, and the SOA of branch-2 is switched ON. The SOAs are operating as fast gates, which allows interchanging the role of branch-1 and branch-2 as the active or standby branches during the guard time of a packet.

The fine synchronizer compensates the residual packet jitter. This is attributed to the residual uncompensated chromatic dispersion and the nonideal equalization of all the optical paths of an optical packet router. One over four fiber delay lines is selected to adjust the packet with respect to a reference clock. The larger dispersion equals the maximum jitter between consecutive packets. The value for the allowable resolution (the amount of uncompensated jitter) is deducted taking into account the correspond-

Fig. 1. Schematic of the optical synchronizer.
ing system tolerance. Typically, we can have the following distribution: 0, 6.2, 12.9, and 26.1 ns. In addition, to suppress the polarization variation that could occur in the WDM synchronizer during the selection of the branch, a distributed feedback (DFB) laser can be used as a probe for a cross-gain modulation wavelength converter to convert all the packets into one unique polarization state. The synchronizer is also adopting a modular architecture, which means that the fine-synchronization part is added only if this is needed, i.e., it is useful only if the switching granularity is at the order of a few microseconds.

3. Practical Implementation of the Optical Synchronizer

A prototype of the synchronizer in Fig. 1 has been implemented for operation at 80 Gbit/s, i.e., a WDM comb of eight wavelengths modulated at 10 Gbit/s each. The setup was mounted onto five boards with dimensions of 360×400 mm². The coarse and fine synchronizers are shown in photos of Figs. 2(a) and 2(b), respectively, while a photo of the front end of the prototype is shown in Fig. 3. Regarding the coarse synchronizer, branch-1 resides in board #1 and it consists of nine optomechanical switches (two 1×2 switches at the input/output of the cascade and seven 2×2 switches) with switching time ~1 ms and insertion loss <0.5 dB. The length of FDL segments have a distribution from 8 to 1024 ns (e.g., in the latter case the fiber segment is 200 m in length). When transistor–transistor logic (TTL) voltage is applied to the switches, the selected total optical delay ranges between 0 and 2048 ns, which is equivalent to the total duration of two packets (packet duration equivalent to 1 μsec).

Similarly, branch-2 resides in board #2. This board also includes the two input couplers of zero, i.e., a 10/90 power-coupler for tapping out a part of the WDM signal that aims to feed the electronic control of the coarse synchronizer, and a second 50/50 coupler for equally splitting up the power between branch-1 and branch-2. Board #3 incorporates two clamped-gain SOAs (G ~ 10 dB, noise figure (NF) = 10 and 12 dB, respectively, and switching time ~1 ns) for selecting the active and standby branches, the 50/50 coupler for combining the two paths, and the erbium-doped fiber amplifier (EDFA) for signal amplification before the demultiplexer. In board #4 the fine synchronizer is implemented. This is composed of a 10/90 coupler, for directing part of the signal to the electronic control, a 4×4 coupler to distribute the signal on four different FDLs (6 to 26 ns), four SOAs to select one of the four delays, and a 4×1 coupler for combining the outputs from the four delay lines. Board #5 incorporates the electronic control circuitry for the coarse synchronizer. This includes an optoelectronic conversion stage followed by a packet arrival rate detection circuitry. In the latter, the registration of the arrival times of the packets is based on a flag that is inserted as a preamble at the beginning of the packets with an effective data rate of 622 Mbit/s. Details for the controller are given in the next section.

Fig. 2. Photo of the coarse synchronizer (a) and fine synchronizer (b).
3.A. Controller
An overview of the controller is shown in Fig. 4. The design of the controller was based on an ECL phase detector circuit with two outputs. The phase detector detects the rising time of the pulse of the incoming packet rhythm, compares this with the local clock, and gives as output a pulse having a duration equal to the time between the arrivals of the two edges. If the phase delay measured is positive, then the pulse is given from the positive output, while the negative stays logically low. If the phase delay is negative, the process is reversed. To detect the rising edge of the rate for the incoming packet, a flag designated with a frequency equal to one quarter of the data clock is used. Equivalently, an envelope detector can be implemented, instead, for the same purpose.

Those two outputs are combined with an OR/NOR gate, and the output is fed to the “count-enable” input of an ECL counter. The counter counts how many clock edges of a local clock at 622 MHz “fit” in the duration that it is enabled, actually counting the absolute value of the phase difference in multiples of 1.6 ns (1/622 MHz). The sign is acquired with the use of a buffer from the positive output of the phase detector. The reset is used for timing, setting, and resetting purposes.

The measured values are then read with the use of a buffer by a data acquisition system, and a PC was used as the controller of the whole system. Because thermal variations are very slow varying stochastic phenomena, the speed of the PC proved to be sufficient. An algorithm was developed that reads the delay, calculates the new
active path, then controls the slow switches of the nonactive branch, and then instructs the fast ECL electronics of the system to do the switching of the branches in a synchronous and very precise way, during the imminent guard band, so that the flow of the packets is not interrupted.

The synchronizer addresses an initial delay of 1024 ns, which is exactly the middle of its dynamic range, for a complete synchronized input (for phase difference=0). When it has to compensate positive delay it adds more delay to the paths, while for negative delay it subtracts delay from the paths. We must stress that bit-synchronization is not required, since it is done at the edge node, burst mode receiver.

3.B. Experimental Demonstration of the Synchronizer
The performance of the coarse synchronizer has been evaluated using a WDM comb comprising eight DFB lasers modulated at 10 Gbit/s. In Fig. 5 four different delays equal to 0, 95, 256, and 512 ns are introduced, and the output of branch-1 of the coarse synchronizer is monitored via an oscilloscope. One can observe that the actual position of the guard band has no effect on how efficiently the synchronizer operates, since no distortion of the packet envelope is observed. It is also worth mentioning that during this experiment, the state of the switches is changing manually. Regarding the fine synchronizer, one port introduces no delay, while different FDL lengths have been allocated to the other three. In particular, compared with the shortest path, the other three ports introduce delays that equal to 6.2, 12.9, and 26.1 ns.

Finally, using the complete setup with both the coarse and the fine synchronizers, BER measurements were carried out. Compared to the back-to-back configuration, the penalty at BER=10^{-9} was measured for different delays of branches 1 and 2. The results are shown in Fig. 6. The penalties were between 0.1 and 1.5 dB, and they were

![Fig. 5. Operation of the proposed optical synchronizer.](image)

![Fig. 6. Power penalty for the rack-mounted 80 Gbit/s experiment.](image)
relatively independent of the delay. Branch-1 penalty is about 1 dB more than branch-2. The extra penalty is attributed to the higher NF of the SOA in branch-1 (12 dB versus 10 dB). Nevertheless, there are commercially available devices with lower NF (typically around 7 dB), so this degradation can be minimized. Simulation results indicate that a synchronizer of 320 Gbit/s can be constructed with no additional penalty. To ensure low performance degradation when cascading the optical router switching matrix after the optical synchronizer, 3R all-optical regeneration is mandatory. Also, the deployment of a wavelength conversion in the fine synchronizer ensures no performance degradation due to the random polarization state of the packets when these are launched into the all-optical regenerator (which is generally based on cross-phase wavelength converters that are sensible to the polarization state).

4. Conclusions
An all-optical synchronizer suitable for optical packet routers, where synchronization only at the packet level like in [1] is necessary, has been described. The proposed synchronizer prototype has been rack-mounted, and its performance has been experimentally evaluated. The coarse (respectively fine) synchronizer has a resolution of 8 ns (respectively 6 ns) and a maximum delay of 2048 ns (respectively 26 ns). The BER measurements that were made at 80 Gbit/s for a WDM comb of eight wavelengths at 10 Gbit/s demonstrated a superior performance with very low system penalties (~1 dB). In addition, simulation results indicated that a synchronizer of 320 Gbit/s (32 × 10 Gb/s) could be constructed with negligible sensitivity penalty. This paper demonstrates that an all-optical packet synchronizer can be realized with commercially available components. The proposed subsystem provides a solution to all practical synchronization issues of synchronous optical packet switching.

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References